

PATENT SPECIFICATION

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DRAWINGS ATTACHED

1 259 268

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(54) DIGITAL PARALLEL TO SERIAL CONVERTER

SPECIFICATION NO. 1, 259, 268

By a direction given under Section 17 (1) of the Patents Act 1949 this application proceeded in the name of THE SINGER COMPANY, a Corporation organised and existing under the laws of the State of New Jersey, United States of America, of 321 First Street, Elizabethport F, New Jersey, United States of America.

THE PATENT OFFICE

R 7026/8

15 a circuit arrangement which converts digital words of a number of binary bits to a continuous stream of binary bits regardless of a variation of the sequential rate of the incoming words.

20 One of the primary problems encountered in digital parallel to serial converters is that of timing the transfer of a number of bits appearing simultaneously on an equal number of lines into a serial stream of bits on a single line. In conjunction with this problem, digital parallel to serial converters 25 known in the past have had the problem of providing a continuous stream of information in serial form without any discontinuities therein. These difficulties arise from the fact that the sequential rate of the incoming words varies over a small range, which variation is primarily due to a change 30 in the speed of the storage media from which the incoming words are retrieved.

35 Because of these problems of prior-known parallel to serial converters, various disadvantages are evident in specific applications of such converters. An example of such a specific application is the conversion of parallel-serial binary data recorded on a 40 rotating magnetic memory to a serial stream of binary bits for display on a television raster. A video signal for the television raster display is formed of the serial stream of bits which must remain continuous regardless of any variation in the speed of 45 the rotating memory, since any discontinuity in the video signal will appear as a repetitive pattern in the display.

It is an object of the present invention

[Price 25p]

ter gates and including an oscillator for generating gating signals at a predetermined rate to transfer the information from parallel form in said register into serial form, 65 means responsive to said gating signals and to said timing pulses for developing an error signal in accordance with the difference between said first rate and said predetermined rate, said generating means being responsive 70 to said error signal for altering said predetermined rate by controlling the frequency of said oscillator.

The oscillator may comprise a flip-flop, a first gate having one input connected to one 75 output of said flip-flop and an output connected to one input of said flip-flop, and a second gate having one input connected to another output of said flip-flop and an output connected to another input of said flip-flop, the other input of each of said gates 80 being connected to a source of voltage.

An embodiment of the present invention will now be described by way of example, with reference to the accompanying drawings, in which:— 85

Fig. 1 is a block diagram of a digital parallel to serial converter constructed in accordance with the present invention;

Fig. 2 illustrates several important waveforms useful in understanding the principles of the present invention; 90

Fig. 3 is a partial block and partial schematic diagram of the oscillator circuit illustrated in Fig. 1; 95

Fig. 4 is a block diagram of the counter illustrated in Fig. 1;

Fig. 5 is a partial block and partial schem-

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 G4C 1D 1F 2G 2JX 2N 2Q



(54) DIGITAL PARALLEL TO SERIAL CONVERTER

(71) We, SINGER-GENERAL PRECISION, INC., a corporation organised and existing under the laws of the State of Delaware, United States of America, of Binghamton, New York 13902, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a digital parallel to serial converter, and more particularly to a circuit arrangement which converts digital words of a number of binary bits to a continuous stream of binary bits regardless of a variation of the sequential rate of the incoming words.

One of the primary problems encountered in digital parallel to serial converters is that of timing the transfer of a number of bits appearing simultaneously on an equal number of lines into a serial stream of bits on a single line. In conjunction with this problem, digital parallel to serial converters known in the past have had the problem of providing a continuous stream of information in serial form without any discontinuities therein. These difficulties arise from the fact that the sequential rate of the incoming words varies over a small range, which variation is primarily due to a change in the speed of the storage media from which the incoming words are retrieved.

Because of these problems of prior-known parallel to serial converters, various disadvantages are evident in specific applications of such converters. An example of such a specific application is the conversion of parallel-serial binary data recorded on a rotating magnetic memory to a serial stream of binary bits for display on a television raster. A video signal for the television raster display is formed of the serial stream of bits which must remain continuous regardless of any variation in the speed of the rotating memory, since any discontinuity in the video signal will appear as a repetitive pattern in the display.

It is an object of the present invention

[Price 25p]

to obviate or mitigate the above disadvantages. 50

According to the present invention there is provided a digital parallel to serial converter, comprising a register disposed for receiving information in parallel format at a first rate which is susceptible to variation, said information also including timing pulses indicative of said first rate, a plurality of transfer gates each having one input connected to a respective output of said register, generating means coupled to said transfer gates and including an oscillator for generating gating signals at a predetermined rate to transfer the information from parallel form in said register into serial form, means responsive to said gating signals and to said timing pulses for developing an error signal in accordance with the difference between said first rate and said predetermined rate; said generating means being responsive to said error signal for altering said predetermined rate by controlling the frequency of said oscillator. 55 60 65 70

The oscillator may comprise a flip-flop, a first gate having one input connected to one output of said flip-flop and an output connected to one input of said flip-flop, and a second gate having one input connected to another output of said flip-flop and an output connected to another input of said flip-flop, the other input of each of said gates being connected to a source of voltage. 75 80

An embodiment of the present invention will now be described by way of example, with reference to the accompanying drawings, in which:— 85

Fig. 1 is a block diagram of a digital parallel to serial converter constructed in accordance with the present invention;

Fig. 2 illustrates several important waveforms useful in understanding the principles of the present invention; 90

Fig. 3 is a partial block and partial schematic diagram of the oscillator circuit illustrated in Fig. 1; 95

Fig. 4 is a block diagram of the counter illustrated in Fig. 1;

Fig. 5 is a partial block and partial schem-

atic diagram of the clock and flip-flop circuits illustrated in Fig. 1;

Fig. 6 is a schematic diagram of the filter circuit illustrated in Fig. 1;

5 Fig. 7 is a block diagram of the decoder illustrated in Fig. 1;

Fig. 8 is a partial block and partial schematic diagram of the data strobe circuit illustrated in Fig. 1;

10 Fig. 9 is a block diagram of the register illustrated in Fig. 1;

Fig. 10 is a block diagram of the transfer gates illustrated in Fig. 1; and

15 Fig. 11 illustrates a number of waveforms useful in understanding the transfer of digital words in the form of parallel binary bits into a continuous stream of serial binary bits and applicable to the converter illustrated in Fig. 1.

20 Like reference numerals throughout the various views of the drawings are intended to designate the same or similar structures.

With reference to Fig. 1, there is shown a digital parallel to serial converter constructed in accordance with the present invention. As shown therein, a storage unit 12, which may be a magnetic drum or the like, continuously supplies digital words in parallel form to an N-bit register 14. A data-strobe circuit 16 enables the register 14 to receive the digital data from the storage unit 12. Once the information is received in the register 14, it is available on output lines 14a, 14b—n for being transferred into a serial stream of information. A plurality of transfer gates 18 (N of which are illustrated) have respective inputs thereof connected to the output lines 14a, 14b—n. By enabling the individual transfer gates 18 in succession, the information contained on the lines 14a, 14b—n is made available on an output line 20 in a serial stream. It can readily be appreciated that the timing of the enabling or gating pulses to the respective transfer gates 18 is of critical importance if it is desired to provide a continuous stream of serial binary bits on the output line 20. As previously mentioned, the sequential rate of the incoming words from the storage unit 12 may vary slightly resulting in a discontinuity in the stream of serial binary bits available at the output of the transfer gates 18.

25 The present invention obviates or mitigates this discontinuity problem by the provision of a phase-locked loop in the circuit which supplies the enabling or gating pulses to the transfer gates 18. In particular, a voltage-controlled oscillator 22 is connected to a counter 24, which counter effectively divides the output of the oscillator 22 by a predetermined factor. An output of the counter 24 is connected to a decoder 26 which supplies gating pulses to the individual transfer gates 18, and another output

of the counter is employed for triggering the data-strobe circuit 16.

One of the storage tracks in the storage unit 12 contains timing information which is supplied to a clock circuit 28, the timing information being synchronized with the transmission of information from the storage unit 12 to the register 14, and the clock circuit 28 generates a series of clock pulses in response to the timing information from the storage unit 12.

70 A flip-flop 30 is responsive to an output from the counter 24 and to the timing pulses generated by the clock circuit 28, and as a result, the output waveform of the flip-flop 30 is a square wave whose DC average value is proportional to the phase error between the incoming timing pulses from the clock circuit 28 and the positive-going edges of the last counter stage in the counter 24. The square wave output of the flip-flop 30 is filtered by a filter circuit 32 which produces a DC error voltage which is supplied to the oscillator 22 to control the frequency thereof.

75 The waveforms illustrated in Fig. 2 are useful in understanding the open-circuit operation of the phase-locked loop including the oscillator 22, the counter 24, the clock circuit 28, the flip-flop 30, and the filter circuit 32. As shown therein, the counter 24 supplies a signal to the flip-flop 30 having a form represented by the waveform 34. The clock circuit 28 supplies timing pulses to the flip-flop 30 having a form represented by the waveform 36. The input to the filter circuit 32 is open circuit. The output of the flip-flop 30 is a square wave having the form represented by the waveform 38, which has a DC average value proportional to the phase error between the incoming timing pulse from the clock circuit 28 and the positive-going edges of the signal from the counter 24. As shown in Fig. 2, every positive transition of the waveform 34 will complement the flip-flop 30 and every pulse from the clock circuit 28 will "SET" the flip-flop 30. The first two positive pulses 38a and 38b of the waveform 38 demonstrate the pulse width which is obtained during the condition when the oscillator 22 is providing the desired frequency output. The positive pulses 38c and 38d of the waveform 38 demonstrate the pulse width which is obtained during a condition of the output frequency of the oscillator 22 being less than desired, and the positive pulses 38e and 38f of the waveform 38 demonstrate the pulse width which is obtained during conditions when the output frequency of the oscillator 22 is greater than that desired.

Fig. 3 illustrates — in partial block and partial schematic diagram form — the oscillator 22 illustrated in Fig. 1. The oscillator

22 is basically an astable multivibrator formed of a flip-flop 40 and two logical inverting (NOR) gates 42. The switching threshold, and thus the delay time, of the gates 42 is controlled by the voltage supplied at an input 44. The voltage at the input 44 is partially developed by a voltage divider network including a potentiometer 46 having the variable contact arm thereof connected to the input 44, and partially by a voltage which is proportional to the DC average value of the signal at the output of the flip-flop 30 developed by the filter circuit 32 and supplied to a terminal 48 which is connected to the input 44. One of the gates 42 has an output connected to the "SET" input of the flip-flop 40 and has an input connected through a resistor 49 to the "1" output of the flip-flop 40. The other of the gates 42 has an output connected to the "RESET" input of the flip-flop 40 and has an input connected through a resistor 50 to the "0" output of the flip-flop 40. A gate 52 transfers the output of the flip-flop 40 to an output line 54.

The gates 42 are formed of emitter-coupled integrated circuit logic elements which are of the nonsaturating type, whereby the oscillator 22 provides a linear function output with the use of digital elements.

The counter 24 is illustrated in Fig. 4 in block diagram form and includes three flip-flops 56, 58, and 60 and a gate 62. Two inputs of each of the flip-flops 56, 58 and 60 are connected to an input terminal 64 which is connected to an output of the oscillator 22. Outputs 56a, 58a and 60a of the flip-flops are supplied to the decoder 26 of Fig. 1. An output 56b of the flip-flop 56 is connected to one input of the gate 62 and to inputs of the flip-flop 58. The flip-flops 56, 58 and 60 are of the buffered JK type, such that when a "0" level appears at the output 56b, the flip-flop 58 is conditioned to change its state upon the occurrence of a pulse at the terminal 64. An output 58b of the flip-flop 58 is connected to the other input of the gate 62, such that when a "0" level appears at the two inputs of the gate 62, a "0" at the output thereof conditions the flip-flop 60 to alter its state upon the occurrence of a pulse at the terminal 64. An output 60b of the flip-flop 60 is supplied to an input of the data strobe circuit 16 and to an input of the flip-flop 30.

The clock circuit 28 and the flip-flop 30 are illustrated in greater detail in Fig. 5, and as shown therein, the clock circuit 28 includes a pair of flip-flops 66 and 68 which are of the buffered JK type. A timing signal from the drum memory storage unit 12 is supplied to an input of the clock circuit at a terminal 70 which is connected to one input of the flip-flop 66. The flip-

flop 66 is conditioned upon the occurrence of a negative-going edge and is triggered upon the subsequent occurrence of a positive-going edge. An RC time-constant circuit 72 is connected at an output of the flip-flop 66 and provides a time delay reset pulse at a reset input 74. An appropriate output from the flip-flop 66 conditions and triggers the flip-flop 68 to provide an output pulse to the "SET" input of the flip-flop 30. An RC time constant circuit 76 is connected between an output of the flip-flop 68 and the "RESET" input thereof to control the pulse width of the signal supplied to the flip-flop 30. The JK inputs of the flip-flop 30 are connected to the output 60b of the counter circuit 24 (see Fig. 4) and an output of the flip-flop 30 is provided on a line 78 to the filter circuit 32.

The filter circuit 32 is illustrated in Fig. 6 wherein an output of the flip-flop 30 is supplied on the line 78 is connected to an input of the filter circuit 32 at a terminal 80. The filter circuit 32 is essentially formed of an operational amplifier which is provided with capacitive feedback to perform an integration. In particular, the input terminal 80 is connected through a resistor 82 to the base of a transistor 84. The collector of the transistor 84 is connected to ground by means of a resistor 85 and the emitter thereof is connected to negative voltage by means of a resistor 86. A transistor 87 is connected between ground potential and the emitter of the transistor 84 and a voltage V is connected to the base of the transistor 87.

The collector of the transistor 84 is connected to the base of a transistor 88 having the collector thereof connected to ground potential. The emitter of the transistor 88 is connected through a resistor 89 to a source of negative voltage. In addition, the emitter of the transistor 88 is connected through a resistor 90 and a capacitor 92 in parallel to the base of the transistor 84. A capacitor 93 is connected between the emitter of the transistor 88 and the source of negative potential. An output from the filter circuit 32 is provided through a resistor 94. In operation, the square wave signal supplied at the terminal 80 develops a DC signal at the output of the filter circuit 32 which is proportional to the average value of the square wave input signal.

The decoder circuit 26 is illustrated in Fig. 7 and includes a plurality of gates 95, 96 and 97. Respective outputs 56a, 58a, and 60a of the counter illustrated in Fig. 4 are connected to respective input terminals 95a, 96a and 97a, respectively. The outputs appearing on the lines 95b, 96b and 97b are of the same polarity as the input signal to the respective gates, while the outputs 95c, 96c and 97c are of opposite polarity to the signal supplied at the inputs of the re-

spective gates. As a result, the signals appearing on the outputs of the gates 95, 96 and 97 provide a 3 bit digital word which is employed for enabling the transfer gates 18.

The data strobe circuit 16 is illustrated in Fig. 8. A gate 98 is provided with three inputs which are connected to the output lines 95c, 96c and 97c of the decoder illustrated in Fig. 7. Only when each of the inputs to the gate 98 is a "0", will the output on the line 100 be a "0". The data strobe circuit 16 also includes a flip-flop 102 having an input connected to the output line 60b of the counter illustrated in Fig. 4. An RC time constant circuit 104 is connected between an output of the flip-flop 102 and a "RESET" input thereto to control the pulse width at the output. The output of the flip-flop 102 is connected through a pair of gates 106 which perform an inversion of the signal and supply an output on lines 106a and 106b.

The register 14 is illustrated in greater detail in Fig. 9. A plurality of pairs of gates 108—115 are disposed for receiving a respective bit of information at their respective *a* input terminal and the complement of a respective bit at their *b* input terminal. The gate 108 is enabled by a pulse applied to a terminal 110 which is connected to the output line 100 in Fig. 8. Gates 109, 110 and 111 are enabled by a pulse applied to a terminal which is connected to the output line 106a in Fig. 8. In addition, gates 112, 113, 114 and 115 are enabled by a pulse supplied to a terminal 114 which is connected to the output line 106b in Fig. 8.

The digital word impressed on the input terminals of the gates 108—115 is transferred to a plurality of flip-flops 117—124 upon the occurrence of an enabling pulse at the input of the gates 108—115. As soon as the information is entered into the flip-flops 117—124, it is available at output terminals 126—133 thereof.

The transfer gates 18 are illustrated in greater detail in Fig. 10. As shown therein, a plurality of gates 135—142 are each provided with four inputs, three of which are connected to respective outputs of the decoder 26, and the fourth of which is connected to a respective one of the output terminals 126—133 of the register 14. The outputs of each of the gates 135—142 are transferred through a respective one of gates 145—152 upon the occurrence of an enabling signal supplied at a terminal 154. The outputs of the gates 145—152 are connected together and to an input of a gate 156 which provides a true and a complement of the information on output lines 158 and 160, respectively.

The operation of the binary parallel to

serial converter disclosed herein can be better understood with reference to Fig. 11 which contains an illustration of several waveforms, denoted A to N, appearing throughout the circuitry. Figs. 11A—H represent typical bits of information which are retrieved from the storage unit 12 supplied to the register 14. Accordingly, the first word of information supplied to the register 14 would consist of the binary bits 10101100.

The waveform of the output of the data strobe circuit 16 is illustrated in Fig. 11-I and occurs during the first count in a count cycle of the counter circuit 24. This output appears on the lines 106a and 106b in Fig. 8. Because of the specific connection of the gate 98 to the output of the decoder 26, an output pulse is provided on the line 100 during the eighth count of a count cycle of the counter 24. With reference to Fig. 10, information is gated through the gates 135—142 in succession, with information being gated through the gate 135 during a first count cycle, information being gated through the gate 136 during a second cycle, information being gated through gate 137 during a third count cycle, etc. Accordingly, when information is being gated through the gate 142 during the eighth count, information is being entered into the flip-flop 117 (see Fig. 9). In addition, when information is being gated through the gate 135 during the first count of the count cycle, information is being entered into the registers 118—124.

The waveforms illustrated in Fig. 11J, L and M correspond with the waveforms illustrated in Fig. 2. The output of the oscillator 22 is illustrated in Fig. 11K, and the serial stream of information on the line 158 in Fig. 10 is illustrated in Fig. 11N.

From a consideration of the waveform illustrated in Fig. 11, it can be appreciated that the serial stream of information on the output lines 158 and 160 is initiated upon the occurrence of a data strobe pulse. The data strobe pulse from the output lines 106a and 106b in Fig. 8 occurs during a first time slot of a counting cycle of the counter 24, while the data strobe pulse on the output line 100 occurs in the previous time slot of the counting cycle. Accordingly, information is entered during a first time slot of the counting cycle into the gates 109—115 and information is transferred to the output lines 158 and 160 from the gate 135 during the same time slot of the count cycle. During the next six time slots of the counting cycle, information is transferred from the registers 109—114 through respective ones of the gates 136—141 in sequence to the output lines 158 and 160. During the eighth time slot of the count cycle, information is transferred into the flip-flop 117

through the gates 108 and is transferred onto the output lines 158 and 160 through the gate 142. Any change in the count frequency due to a variation in drum speed will be corrected by the phase-locked loop including the oscillator 22, the counter 24, the clock 28, the flip-flop 30, and the filter 32.

The above-described digital parallel to serial converter is capable of supplying a continuous stream of serial binary bits regardless of a small variation of the sequential rate of the incoming word and is therefore suitable for providing a television raster display of digital video information. By virtue of the phase-locked loop which is responsive to an output from the reference oscillator and is further responsive to clock pulses the output frequency of the oscillator is controlled.

WHAT WE CLAIM IS:—

1. A digital parallel to serial converter, comprising a register disposed for receiving information in parallel format at a first rate which is susceptible to variation, said information also including timing pulses indicative of said first rate,

a plurality of transfer gates each having one input connected to a respective output of said register,

generating means coupled to said transfer gates and including an oscillator for generating gating signals at a predetermined rate to transfer the information from parallel form in said register into serial form, means responsive to said gating signals and to said timing pulses for developing an error signal in accordance with the difference between said first rate and said predetermined rate,

said generating means being responsive to said error signal for altering said predetermined rate by controlling the frequency of said oscillator.

2. A parallel to serial converter as claimed in claim 1, wherein said developing means generates a signal which is proportional to the phase disparity between an output pulse of said oscillator and one of said timing pulses.

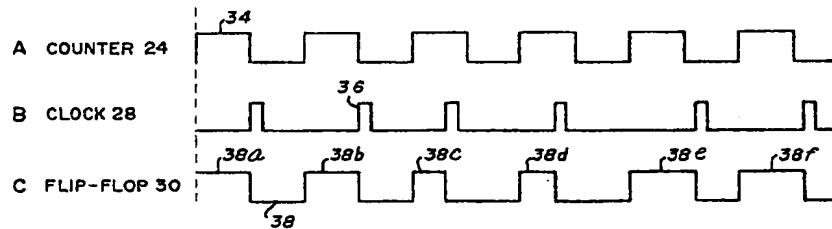
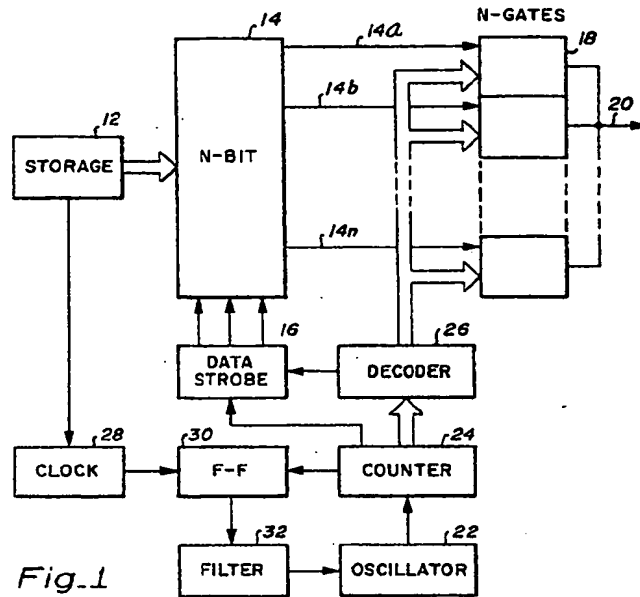
3. A parallel to serial converter as claimed in claim 2, wherein said developing means includes a bistable device having one input coupled to an output of said oscillator and another connected to receive said timing pulses, and means for generating a D.C. voltage proportional in amplitude to the average voltage of an output signal of said bistable device, said oscillator being controlled in accordance with said DC voltage.

4. A parallel to serial converter as claimed in claim 3, wherein said generating means includes frequency-dividing means for frequency dividing an output of said oscillator.

5. A parallel to serial converter as claimed in claim 4, wherein said oscillator includes a flip-flop, a first gate having one input connected to one output of said flip-flop and an output connected to one input of said flip-flop, and a second gate having one input connected to another output of said flip-flop and an output connected to another input of said flip-flop, the other input of each of said gates being connected to a source of voltage to control the frequency of said flip-flop.

6. A digital parallel to serial converter substantially as hereinbefore described with reference to the accompanying drawings.

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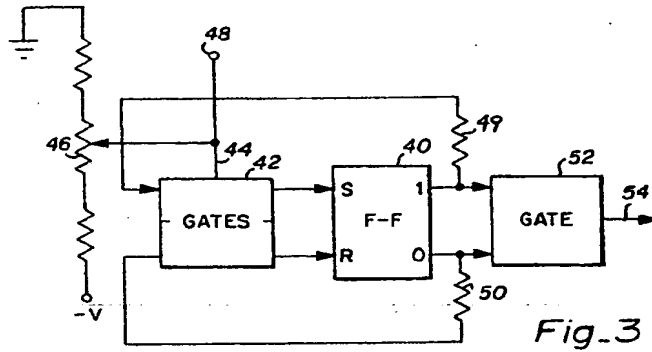


Fig. 4

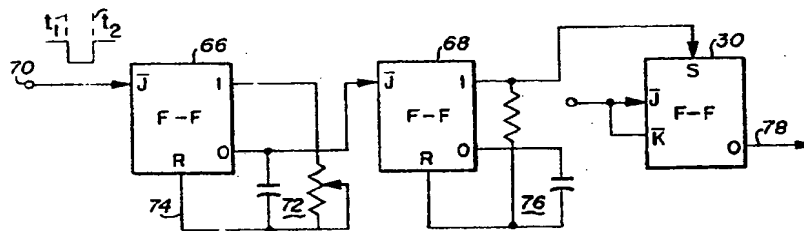
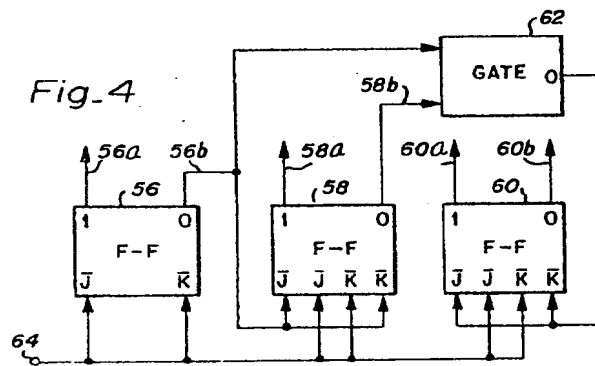


Fig. 5

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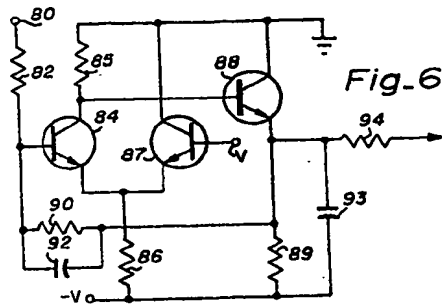


Fig-6

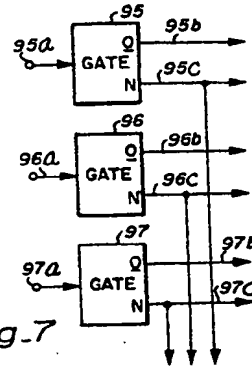


Fig-7

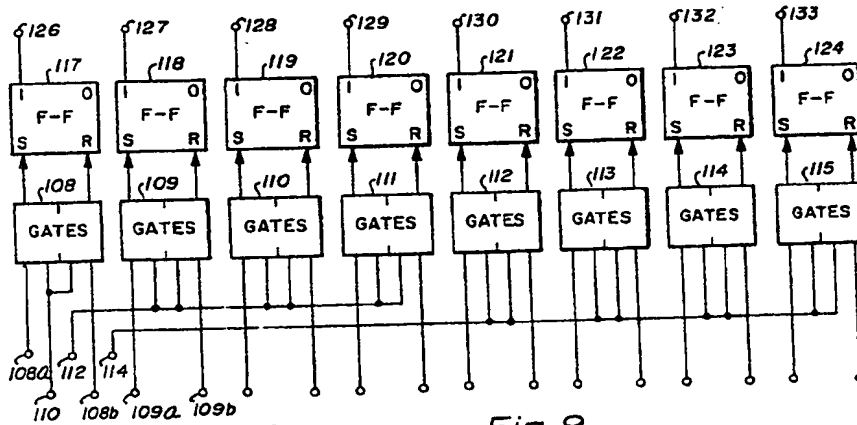


Fig-9

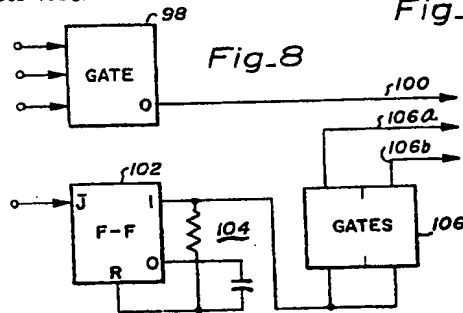


Fig-8

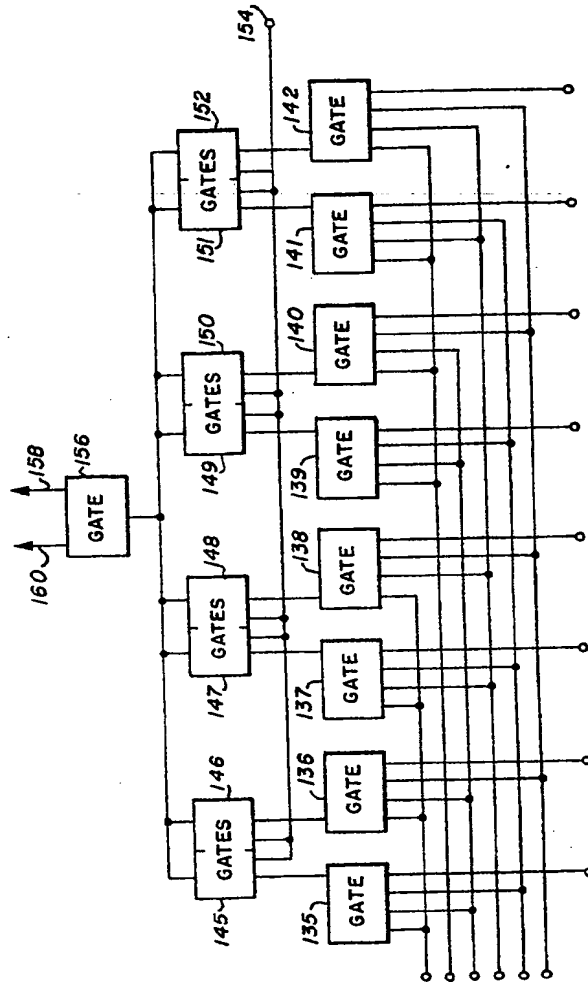


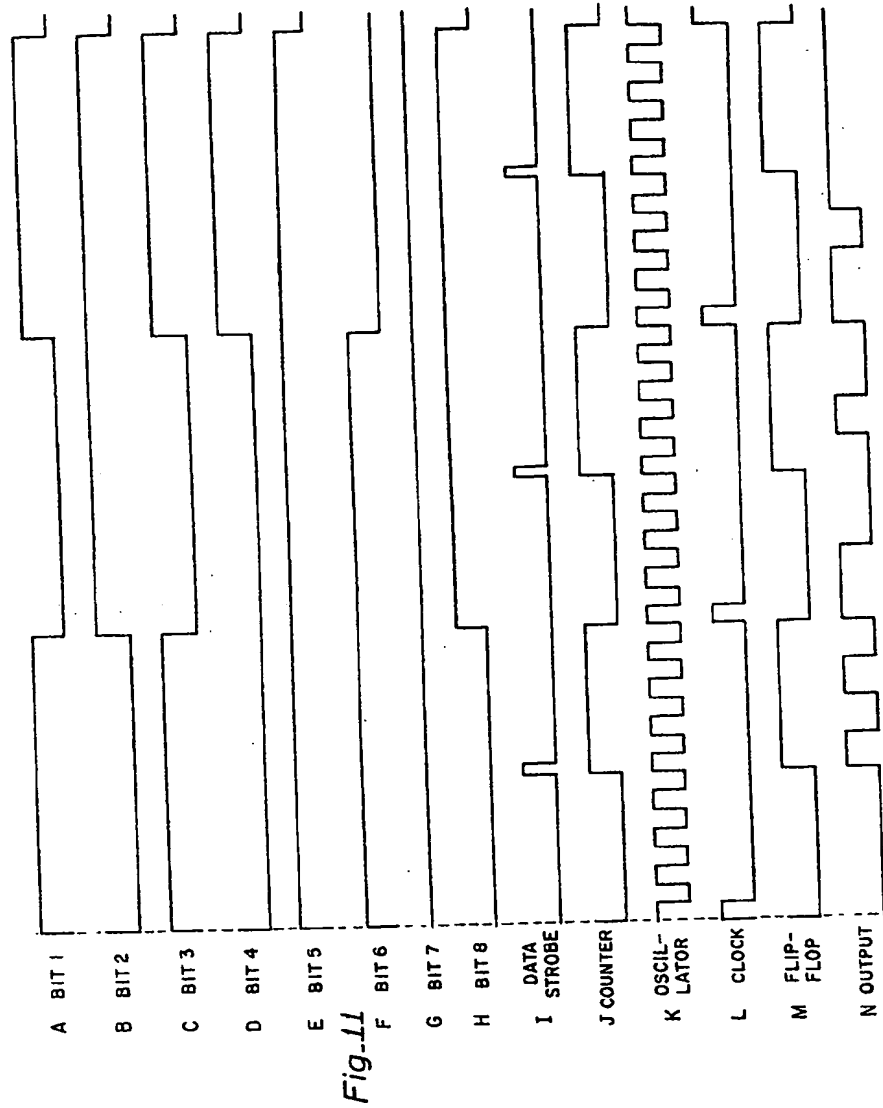
Fig-10

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